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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
TRUJILLO, JAMES K

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2116	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/746,168	Applicant(s) SARANGI ET AL.	
	Examiner James K. Trujillo	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Amendment A dated 2/20/04.

2. Claims 1-20 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Applicant's arguments with respect to claim 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 13 recites the limitation "configuration signal logic" in line 1 and 3 as well as reciting "front-end logic" in line 2. There is insufficient antecedent basis for these limitations in the claim.

Claim Objections

7. Claims 2-4, 12 and 13 are objected to because of the following informalities:

a. As to claim 2-4, "fuse block voltage" in each claim should be changed to "supply voltage" because of amendments to claim 1.

b. As to claim 12, "configuration signal logic" on line 1 of the claim should be changed to "control signal" to prevent a lack of antecedent basis.

c. As to claim 13, "configuration signal logic" on lines 1 should be changed "control signal" and "the configuration signal logic" on line 3 should be changed to "logic for the control signal" and "front-end logic" on line 2 should be changed to "processor" to prevent a lack of antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Gibson et al., U.S. 6,601,167.

10. As to claim 11, Gibson teaches an apparatus comprising:

a. a processor (processor 14) to receive a control signal (signal from boot load) [col. 3 lines 46-51]; and

b. inhibit booting up (by the boot loader) in response to receiving the control signal [col. 3 lines 46-51].

Specifically, the boot loader of Gibson controls whether the processor boots or not. Gibson must use a control signal to inhibit the booting of the processor.

11. As to claim 12, Gibson taught the apparatus according to claim 11, as described above. Gibson further teaches where in the control signal inhibits booting up of the processor for a period of time [col. 3 lines 46-51 et seq.]. Specifically, the boot loader of Gibson waits until a PWRGOOD signal is sensed and allows the processor to boot up.

12. As to claim 13, Gibson taught the apparatus according to claim 11, as described above. Gibson further teaches wherein the control signal is coupled to the processor to inhibit booting of the processor (must be coupled for inhibit to take place) for a period of time after logic for the control signal has power (the boot loader must be power to determine whether or not boot should take place and must be powered to inhibit booting) [col. 3 lines 46-51 et seq.].

13. Claims 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Witowski et al., U.S. 5.446,403.

14. As to claim 11, Witowski taught an apparatus comprising:

a. a processor (CPU 77) to receive a control signal (a system reset); and

b. to inhibit booting up in response to receiving the control signal [figure 7 and corresponding text].

15. As to claim 12, Witowski taught the apparatus according to claim 11, described above. Witowski further taught wherein the configuration signal logic is to inhibit booting up of the processor for a period of time [figures 7 and 8].

16. As to claim 13, Witowski taught the apparatus according to claim 11, described above. Witowski further taught wherein the control signal is coupled to the processor to inhibit booting

up of the processor for a period of time after the control signal has power (the reset causes the boot and the reset is powered only after receiving the delayed power good signal) [figures 5-8].

Claim Rejections - 35 USC § 103

17. Claim 1-5, and 14-15 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Capps, Jr. et al., U.S. Patent 5,764,529 in view of Witowski, U.S. Patent 5,446,403.

18. As to claim 1, Capps teaches an apparatus comprising:

a. a voltage regulator (102) and clock generator (101) to send a processor voltage (203) and a processor clock respectively (201) [figures 1 and 1A];

b. a processor (microprocessor 100) coupled to the voltage regulator to the processor voltage and clock generator to receive the processor clock respectively; and

c. a fuse block programmed with the voltage configuration signal and a frequency configuration signal to specify the processor voltage and the processor clock frequency.

Capps does not expressly disclose a *control signal coupled to the processor, the voltage regulator, and the clock generator to prevent the processor from receiving the processor voltage and the processor clock until* the fuse block programmed with a voltage configuration signal and a frequency signal to specify the processor voltage and processor clock frequency, respectively, *is determined to have a proper supply voltage level* [emphasis added].

Specifically, Capps is silent with respect to preventing the processor from receiving the processor voltage and processor clock.

Witowski teaches an apparatus that has a control signal (delayed POWERGOOD signal) coupled to a processor (CPU 77), a voltage regulator (power supply 72) and a clock generator (clock generator 76) [Figure 9]. Witowski further teaches that the control signal prevents the processor from receiving the processor voltage and the processor clock until it is determined to have a proper supply voltage [figure 7 and col. 4 line 62 et seq.].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Capps by implement the control signal to prevent the processor from receiving the processor voltage and the processor clock as taught by Witowski (wherein the voltage regulator 102 of Capps would issue a POWERGOOD signal as the power supply 72 of Witowski). One of ordinary skill in the art would have been motivated to make the modification because Witowski teaches that it is desirable for the voltage supply to be stable before applying both the voltage and clock [col. 1 lines 24-31 and col. 2 lines 48-47].

19. As to claim 2, Capps together with Witowski taught the apparatus according to claim 1, described above. Capps further teaches that the voltage regulator is coupled to send the supply voltage () to the processor (which would correspond to the voltage according to the fuse block). Witowski teaches that the control (PWRGOOD signal) is sent to the processor and to the clock generator (clock generator 76).

20. As to claim 3, Capps together with Witowski taught the apparatus according to claim 1, as described above. Capps further teaches a second voltage regulator (power supply 140) coupled to send the fuse block voltage to the processor [figure 1]. Witowski further taught sending the control signal to the first voltage regulator, the processor, and the clock generator [figures 9 and 10].

21. As to claim 4, Capps together with Witowski taught the apparatus according to claim 1, as described above. Capps further taught a second voltage generator (power supply 140) coupled to send the fuse block voltage to the processor [figure 1]. Witowski further taught wherein the first voltage regulator is coupled to sense the fuse block voltage and to send the control signal to the processor and the clock generator [figures 9 and 10].

22. As to claim 5, Capps together with Witowski taught the apparatus according to claim 1, as described above. Capps together with Witowski do not expressly disclose a transistor coupled to invert the control signal and sent the inverted control signal to the clock generator. However, one skill in the art would have recognized that the control signal might be used in positive, negative or mixed logic accordingly. That is, the control signal would function the same whether it is or is not inverted. As an example the clock generator as described by Witowski uses an enable input that would be enabled when the control signal is not inverted. One of ordinary skill would recognize that the clock generator having an inverted enable input would have to use a inverted control signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a transistor to invert the control signal because one of ordinary skill would have expected the control signal to function according to type of hardware used.

23. As to claims 14 and 15, Capps together with Witowski taught the claimed apparatus therefore together they also teach the claimed machine-readable medium.

24. Claims 6-10 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Capps in view of Voit, U.S. Patent 6,275,364.

25. As to claim 6, Capps teaches a system comprising:

a. a processor having programmable fuse block programmed (fuses 110-125) with at least one configuration signal [figure 1];

b. logic coupled (clock generator 101 and voltage regulator 102) to the processor to read the configuration signal (using PROC SID 200 and PROC VID 202) and in response to generate a value (using PROC BUS CLOCK and PROC CORE VOLTAGE) specified by the configuration signal [figure 1 and col. 2 line 47 et seq.].

Capps does not expressly disclose a control signal coupled to the processor and the logic to prevent the logic from reading the configuration signal until a predetermined event occurs. Capps does implicitly suggest that the configuration signal be provided before they are read by the logic [col. 5 lines 1-15].

Voit teaches a system that has a control signal coupled to the processor and the logic to prevent the logic from reading the configuration signal until a predetermined event occurs (VID signals reach a predetermined state) [figure 3 and col. 6 lines 6-16]. While not explicit, it would be understood that a control signal must exist to prevent the configuration signal from being read by the VRMs of Voit.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Capp by using a control signal to prevent the configuration signals from being read as taught by Voit. One of ordinary skill in the art would made the modification because it ensure that the correct configuration signals would be read by the logic circuits.

26. As to claim 7, Capps together with Voit taught the system according to claim 6, described above. Capps further teaches that the configuration signal specifies a voltage for the logic to generate.

27. As to claim 8, Capps together with Voit taught the system according to claim 6, described above. Capps together with Voit teach wherein the configuration signal specifies a voltage for the logic to generate. However, one of ordinary skill in the art would have readily recognized that configuration signals using frequency, as taught by Capps, would also benefit by using a control signal as taught by Voit applied to the clock generator rather than a voltage regulator with a reasonable expectation of success.

28. As to claim 9, Capps together with Voit taught the system according to claim 6, as described above. Voit further teaches that the predetermined event is when power to the programmable fuse block is valid and stable (predetermined state is interpreted to be when fuse blocks are valid and stable) [col. 6 lines 6-10]. One of ordinary skill would interpret that the predetermined state would suggest that the VID would valid and stable.

29. As to claim 10 Capps together with Voit taught the system according to claim 6, as described above. Voit further teaches that the predetermined event is when the configuration signal is valid and stable (predetermined state is interpreted to be when fuse blocks are valid and stable) [col. 6 lines 6-10]. One of ordinary skill would interpret that the predetermined state would suggest that the VID would valid and stable.

30. As to claims 16-20, Capps together with Voit taught the system, therefore together they also teach the machine-readable medium.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,327,663 to Isaac et al. This patent teaches a system and method for voltage detection.

U.S. Pat. No. 5,758,170 to Woodward et al. This patent teaches a system for placing a CPU in a hold state prior to transmitting a reset signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703)308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
April 29, 2004

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